CLAIMS

What is claimed is:

1. A method for fabricating an integrated electronic system comprising the steps of:
   (a) providing a plurality of individual semiconductor structures fabricated for capture by an assembly template;
   (b) forming the assembly template for capture of particular ones of the individual semiconductor structures;
   (c) populating the assembly template with the particular ones of the individual semiconductor structures to form a populated assembly template with the particular ones of the individual semiconductor structures on the populated assembly template; and
   (d) bonding at least one of the individual semiconductor structures on the populated assembly template with a host substrate comprising one or more host circuits.

2. The method of Claim 1 wherein at least one of the individual semiconductor structures is formed by a masking and etching process.

3. The method of Claim 1 wherein the assembly template is formed with receptacles and the individual semiconductor structures and the receptacles are formed to be complementary to each other.

4. The method of Claim 3 wherein step (c) is performed through the use of a fluid transport medium.

5. The method of Claim 1 wherein step (d) further comprises the step of aligning the populated assembly template to the host substrate before bonding the at least one individual semiconductor structure to the host substrate.

6. The method of Claim 5, wherein the assembly template and the host substrate have alignment marks and the step of aligning comprises aligning the alignment marks.

7. The method of Claim 1 wherein the step of bonding comprises direct surface bonding, plasma-assisted bonding, plasma-activated bonding, eutectic bonding or gold compression bonding.

8. The method of Claim 1, wherein the host substrate comprises a material from the group consisting of GaAs, InP, SiC, Al_2O_3, Si, SiGe, GaSb, InSb, CdTe, CdZnTe, and InAs.

9. The method of Claim 1, wherein the individual semiconductor structures may comprise one or more structures from the group consisting of capacitors, inductors, diodes, transistors, and integrated circuit modules.

10. The method of Claim 1, wherein step (a) comprises the steps of:
    (a1) growing one or more device layers on a growth substrate wafer;
    (a2) delineating the one or more device layers to provide one or more delineated elements;
    (a3) applying a filler layer over the one or more delineated elements;
    (a4) removing some or all of the growth substrate wafer;
    (a5) patterning the one or more delineated elements to provide one or more individual semiconductor structures of the plurality of individual semiconductor structures; and
    (a6) removing the filler layer to release the one or more individual semiconductor structures.

11. The method of Claim 10, wherein step (a3) includes a step of applying a handle wafer and step (a6) includes a step of removing the handle wafer.

12. The method of Claim 1, wherein step (a) comprises the steps of:

(a1) growing one or more device layers on a growth substrate wafer;

(a2) processing the one or more device layers to provide one or more individually delineated and geometrically shaped semiconductor structures;

(a3) applying a filler layer over the plurality of individually delineated and geometrically shaped semiconductor structures;

(a4) removing some or all of the growth substrate wafer to provide one or more individual semiconductor structures of the plurality of individual semiconductor structures; and

(a5) removing the filler layer to release the one or more individual semiconductor structures.

13. The method of Claim 12, wherein step (a3) includes a step of applying a handle wafer and step (a5) includes a step of removing the handle wafer.

14. The method of Claim 1, wherein step (a) comprises the steps of:

(a1) growing one or more device layers on a growth substrate wafer;

(a2) applying a polymer layer on top of the one or more device layers;

(a3) forming geometric shapes in the polymer layer;

(a4) delineating the one or more device layers under the geometric shapes to provide one or more delineated and patterned semiconductor structures;

(a5) applying a filler layer over the one or more delineated and patterned semiconductor structures

(a6) removing some or all of the growth substrate wafer to provide one or more individual semiconductor structures of the plurality of individual semiconductor structures; and

(a7) removing the filler layer to release the one or more individual semiconductor structures.

15. The method of Claim 14, wherein step (a5) includes a step of applying a handle wafer and step (a7) includes a step of removing the handle wafer.

16. The method of Claim 1, where step (a) comprises the steps of:

(a1) growing one or more device layers on a growth substrate wafer;

(a2) applying a polymer layer on top of the one or more device layers;

(a3) forming geometric shapes in the polymer layer;

(a5) applying a filler layer over the geometric shapes in the polymer layer;

(a6) delineating the one or more device layers to provide the one or more individual semiconductor structures; and

(a7) removing the filler layer to release the one or more individual semiconductor structures.

17. The method of Claim 1, wherein the geometric shapes are alignment structures comprising one or more layers of polymer material.

18. The method of Claim 16, wherein step (a5) includes a step of applying a handle wafer and step (a7) includes a step of removing the handle wafer.

19. The method of Claim 1, wherein step (b) comprises the steps of:

(b1) applying a polymer layer to an assembly substrate wafer; and

(b2) stamping the polymer layer with a stamp wafer to form receptacles in the polymer layer to provide the assembly template.

20. The method of Claim 1, wherein step (b) comprises the steps of:

(b1) providing a silicon wafer;

(b2) masking the silicon wafer; and

(b3) removing the unmasked portions of the silicon wafer to form receptacles in the silicon wafer to provide the assembly template.

21. The method of Claim 20, wherein steps (b2) and (b3) are performed multiple times to provide one or more receptacles having a primary cavity and one or more secondary alignment key structures, the one or more secondary alignment key structures having heights that are less than a depth of the primary cavity.

22. The method of Claim 1, wherein step (d) comprises the steps of:

(d1) positioning the host substrate above the populated assembly template

(d2) aligning the host substrate with the populated assembly template;

(d3) bringing the host substrate into contact with at least one of the individual semiconductor structures on the populated assembly template;

(d4) bonding at least one of the individual semiconductor structures on the populated assembly template to the host substrate using a surface-mounting process; and

(d5) releasing the bonded individual semiconductor structures from the populated assembly template.

23. The method of Claim 1, wherein the host substrate is fabricated to provide one or more wells, each well of the one or more wells fabricated to receive one of the plurality of individual semiconductor structures.

24. The method of Claim 23, the method further comprising the steps of:

providing the host substrate with the one or more host circuits and with one or more window regions, said window regions having window layers over said window regions;

applying a circuit protection layer over said one or more host circuits;

removing said window layers; and

etching said host substrate at said window regions to provide said wells.

25. An integrated electronic system made by the method of Claim 1, wherein at least one of the one or more host circuits comprises a CMOS circuit, an InP-based MMIC, a GaAs-based MMIC, or a Nitride-based MMIC.

26. A method for fabricating an integrated electronic system comprising the steps of:

(a) providing a plurality of semiconductor structures of one or more types, each type of semiconductor structure being fabricated with a corresponding geometric shape;

(b) forming an assembly template, the assembly template having an array of receptacles, each receptacle having a shape complementary to the geometric shape of one type of semiconductor structure;

(c) positioning at least one semiconductor structure of the plurality of semiconductor structures in at least one receptacle of the assembly template, each semiconductor structure being positioned in a receptacle having a shape complementary to the geometric shape of the semiconductor structure; and

(d) bonding at least one of the semiconductor structures in a receptacle of the assembly template to a host substrate having one or more host circuits.

27. The method of Claim 26, wherein step (a) comprises the steps of:

(a1) growing one or more device layers on a growth substrate wafer;

(a2) delineating the one or more device layers to provide one or more delineated elements;

(a3) applying a filler layer over the one or more delineated elements;

(a4) removing at least a portion of the growth substrate wafer;

(a5) patterning the one or more delineated elements to provide one or more semiconductor structures of the plurality of semiconductor structures; and

(a6) removing the filler layer to release the one or more semiconductor structures.

28. The method of Claim 26, wherein step (a) comprises the steps of:

(a1) growing one or more device layers on a growth substrate wafer;

(a2) processing the one or more device layers to provide one or more individually delineated and geometrically shaped semiconductor structures;

(a3) applying a filler layer over the plurality of individually delineated and geometrically shaped semiconductor structures;

(a4) removing at least a portion of the growth substrate wafer to provide one or more semiconductor structures of the plurality of semiconductor structures; and

(a5) removing the filler layer to release the one or more semiconductor structures.

29. The method of Claim 26, wherein step (a) comprises the steps of:

(a1) growing one or more device layers on a growth substrate wafer;

(a2) applying a polymer layer on top of the one or more device layers;

(a3) forming geometric shapes in the polymer layer;

(a4) delineating the one or more device layers under the geometric shapes to provide one or more delineated and patterned semiconductor structures;

(a5) applying a filler layer over the one or more delineated and patterned semiconductor structures

(a6) removing at least a portion of the growth substrate wafer to provide one or more semiconductor structures of the plurality of semiconductor structures; and

(a7) removing the filler layer to release the one or more semiconductor structures.

30. The method of Claim 26, wherein step (a) comprises the steps of:

(a1) growing one or more device layers on a growth substrate wafer;

(a2) applying a polymer layer on top of the one or more device layers;

(a3) forming geometric shapes in the polymer layer;

(a5) applying a filler layer over the geometric shapes in the polymer layer;

(a6) delineating the one or more device layers to provide one or more semiconductor structures; and

(a7) removing the filler layer to release the one or more semiconductor structures.

31. The method of Claim 26, wherein step (b) comprises the steps of:

(b1) providing an assembly template wafer;

(b2) applying a polymer layer to the assembly template wafer;

(b3) fabricating a stamp pattern wafer, the stamp pattern wafer having one or more patterns with generally the same shapes as the geometric shapes of the semiconductor structures; and

(b4) applying the stamp pattern wafer to the polymer layer to provide the array of receptacles.

32 The method of Claim 26, wherein step (b) comprises the steps of:

(b1) providing a silicon wafer;

(b2) masking the silicon wafer; and

(b3) removing the unmasked portions of the silicon wafer to form the array of receptacles in the silicon wafer to provide the assembly template,

wherein steps (b2) and (b3) are performed multiple times to provide one or more receptacles having a primary cavity and one or more secondary alignment key structures, the one or more secondary alignment key structures having heights that are less than a depth of the primary cavity.

33. The method of Claim 26, wherein step (c) comprises the steps of:

(c1) mixing the semiconductor structures with an assembly fluid to form a slurry;

(c2) depositing the slurry on the assembly template to cause each semiconductor structure to self-align in the complementary-shaped receptacle; and

(c3) removing the assembly fluid.

34. The method of Claim 26, wherein step (d) comprises the steps of:

(d1) positioning the host substrate above the assembly template

(d2) aligning the host substrate with the assembly template;

(d3) bringing the host substrate into contact with at least one of the individual semiconductor structures;

(d4) bonding at least one of the individual semiconductor structures to the host substrate using a surface-mounting process; and

(d5) releasing the bonded individual semiconductor structures from the assembly template.

35. The method of Claim 26, wherein the host substrate is fabricated to provide one or more wells, each well of the one or more wells fabricated to receive one of the plurality of individual semiconductor structures.

36. The method of Claim 35, the method further comprising the steps of:

providing the host substrate with the one or more host circuits and with one or more window regions, said window regions having window layers over said window regions;

applying a circuit protection layer over said one or more host circuits;

removing said window layers; and

etching said host substrate at said window regions to provide said wells.

37. The method of Claim 26 wherein step (d) further comprises the step of aligning the assembly template to the host substrate before bonding the at least one individual semiconductor structure to the host substrate.

38. The method of Claim 37, wherein the assembly template and the host substrate have alignment marks and the step of aligning comprises aligning the alignment marks.

39. The method of Claim 26 wherein the step of bonding comprises direct surface bonding, plasma-assisted bonding, plasma-activated bonding, eutectic bonding or gold compression bonding.

40. The method of Claim 26, wherein the host substrate comprises a material from the group consisting of GaAs, InP, SiC, Al_2O_3, Si, SiGe, GaSb, InSb, CdTe, CdZnTe, and InAs.

41. The method of Claim 26, wherein the types of semiconductor structures may comprise one or more structures from the group consisting of capacitors, inductors, diodes, transistors, and integrated circuit modules.

42. An integrated electronic system made by the method of Claim 26, wherein at least one of the one or more host circuits comprises a CMOS circuit, an InP-based MMIC, a GaAs-based MMIC, or a Nitride-based MMIC.